Recent Trends in Power, Control and Instrumentation Engineering, PCIE

A Survey of Processors for Space Applications

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***Abstract*—In recent years the complexity of space- oriented applications has grown dramatically. The amount of processing utilized in spacecrafts has increased. The data rates and volumes produced by both scientific and commercial space missions have increased significantly thus creating an urgent need for better processors. For space applications, high performance and high reliability are the most major issues that become more and more important. Satellites are expensive, computers are unreliable and if failing they will risk the mission. Past space computers were expensive and hard to get, hence the drive to make space computers based on COTS. This paper surveys various approaches to space processors and offers some recommendations. An analysis and survey has been done on various processors regarding radiation hardened, fault tolerant, low power, high performance and also comparison has been done for that processors. Empowered with the analysis of past the future research roadmap is proposed.**

***Index Terms*— High performance, Processors, Reliability, Satellites, Space applications, Temperature.**

I. INTRODUCTION

For space applications, high performance, reliability and temperature are the 3 major indicators that become more and more important for processors designed particularly for space applications. Now, the launching of satellites is for a period of 15-20 years. So, now it is very important to design the electronic circuitry or processors which are reliable, aging and temperature variant, as the temperature in space is so harsh. So, every design needs to carefully design considering all these parameters in order to improve the satellite's reliability .In this paper, survey of space processors has been done. The survey is primarily intended for developers and researchers who are doing work in space applications.

The reliability and aging of satellites are very important today as now the satellites are designed for 15-20 years. So, the electronic components would also be reliable as they have to do processing for a long period of times. Many satellites are unsuccessful because of the reliability and temperature variation. The primary problem is to investigate the reliability and aging of processor for space applications. So, the satellites will be more reliable and the successful launching will be possible.

Space systems operate in an environment whose effects and descriptions are unusual compared with the weather in earth's atmosphere. Engineering new systems to survive and perform in space is still a challenge after more than 40 years of space flight. The space environment, just as any environment on earth, contains phenomena that are potentially hazardous to humans and technical systems; however many of these hazards involve plasma and high energy electrons and ions that are relatively uncommon with in earth's atmosphere. So, there is a great need to survey and develop space systems which must meet their performance requirements regardless of the space weather. So, it is very important to maintain the temperature variations

Grenze ID: 02.PCIE.2015.3.513
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so that the processing of the device will not be degraded. If the temperature variation will not be considered that electronic circuitry performance will be affected and it degrades the satellite. So, this parameter needs more concentration while designing the processors for space applications

Processors for space are required to be tolerant to the following radiation and environmental effects: TID (100- 300 kRad for GEO and beyond, 10-50 kRad for some LEO missions), Latch-up, SEU, SET, SEFI, and temperature cycles. Another reliability issue is the complete and permanent failure of a processor or a critical sub-component. None of the methods surveyed here mitigate such failures, and the common mitigation method is based on deploying spare computers in combination with either a central reconfiguration circuit or a distributed recovery mechanism.

So, the paper is organized as follows: Section II discuss the role of processors in space, section III presents the brief detail of various processors in terms of low power, cost, performance, reliability, aging and radiation hardened and comparison analysis has also been presented. Section IV concluded the survey analysis.

II. Role of Processors in space

Continuous transistor scaling due to the improvements in CMOS devices and manufacturing technologies is increasing processor power densities and temperature thus creating challenges when trying to maintain manufacturing yield rates and devices which are reliable throughout their life time.

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New micro-architecture requires new reliability aware, temperature variant processors that can face these challenges without significantly increasing cost and performance. In space applications high performance, temperature variant and reliability are the three indicators that become more and more important to a processors. As now the launching of satellites is for period of 15-20 years and also the environment in which processors operate in space is particularly harsh. The temperature range over there is very wide extremes. The surfaces exposed to the sun are heated by solar radiations and will rise to very high temperature whereas other side that is not heated will be exceedingly cold. So, the processing will be greatly affected under such circumstances. So, it is very important to survey the processors for space applications and then the techniques will be imposed in order to improve the reliability and aging of processors used in space.

III. Processors architecture and its specifications

Processors for space applications are typically required to achieve the following targets: high performance, low cost, low power dissipation, and reliability. This is sometimes achieved by high integration (for high performance, low cost and low power dissipation) and high tolerance to radiation and environmental effects (for reliability). The problem is that most available processors and integrated systems-on- chip achieve only some of the targets and fail on others. This is indicated below when relative advantages and disadvantages are listed, and exemplified in later sections. The following section surveys the different approaches to this tradeoff.

A. ATMEL Processors

Over the last 16 years, Atmel has steadily built a space microprocessor strategy based on the SPARC® architecture. With worldwide sales of over 3000 flight models featuring the Atmel® TSC695 — and already over 300 flight models with the Atmel AT697 — the Atmel SPARC processor roadmap boasts an unrivalled flight heritage. ATMEL processors include the following: AT697, AT697F, TSC695F, TSC695FL, TSC695F, ATF697FF and many more.

AT697 was the version of a SPARC V8 high performance low power 32-bit architecture. This is highly integrated, high performance 32-bit RISC embedded processor. The implementation is based on the European Space Agency (ESA) LEON2 fault tolerant model. By executing powerful instructions in a single clock cycle, this achieves throughputs approaching 1MIPs per MHz. allowing the system designer to optimize power consumption versus speed. This can be easily studied from figure 1 below. The processor is manufactured using the Atmel 0.18µm CMOS process. It has been espically designed for space applications, by implementing on-chip concurrent transient and permanent error detection and correction.

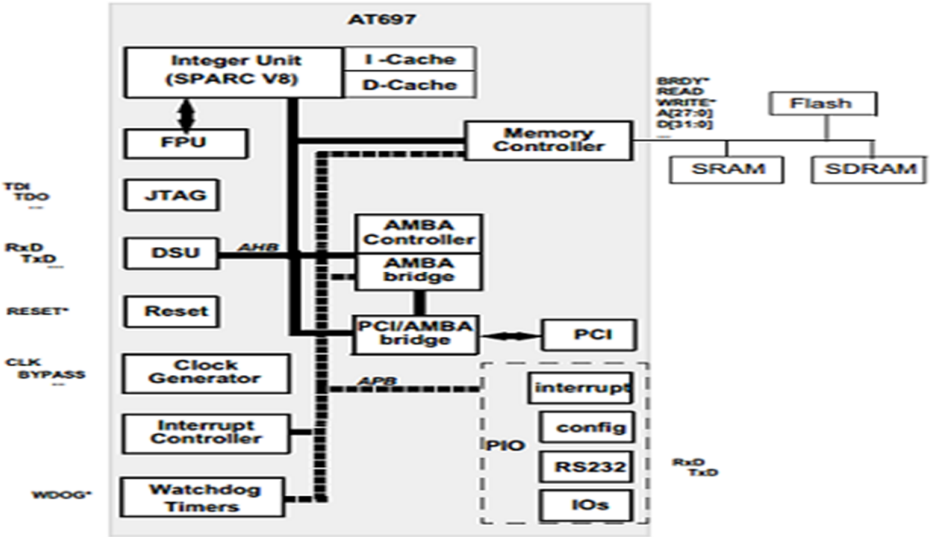

Figure 1. Block Diagram of AT697 [5]

The TSC695F (ERC32 Single-Chip) is a highly integrated, high-performance 32-bit RISC embedded processor implementing the SPARC architecture V7 specification. It has been developed with the support of the ESA (European Space Agency), and offers a full development environment for embedded space applications. The processor is manufactured using the Atmel 0.5 µm radiation tolerant (≥ 300 KRADs (Si)) CMOS enhanced process (RTP). It has been specially designed for space, as it has on-chip concurrent transient and permanent error detection. The TSC695F includes an on-chip Integer Unit (IU), a Floating Point Unit (FPU), a Memory Controller and a DMA arbiter. For real-time applications, the TSC695F offers a high security watchdog, two timers, an interrupt controller, parallel and serial interfaces. Fault tolerance is supported using parity on internal/external buses and an EDAC on the external data bus. The design is highly testable with the support of an On-Chip Debugger (OCD), and a boundary scan through JTAG interface. This is shown in fig.2.

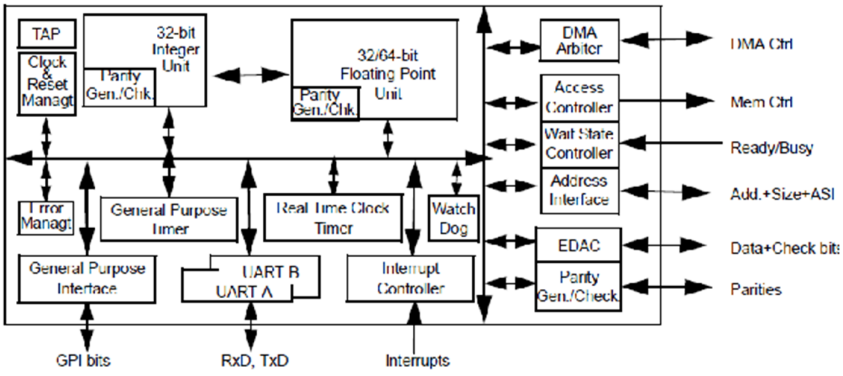

Figure 1. Block Diagram of TSC695F

The TSC695FL (ERC32 Single-Chip) is a highly integrated, high-performance 32-bit RISC embedded processor implementing the SPARC architecture V7 specification. This is specified in figure 3. It has been developed with the support of the ESA (European Space Agency), and offers a full development environment for embedded space applications. The processor is manufactured using the Atmel 0.5 µm radiation tolerant (≥ 300 KRADs (Si)) CMOS enhanced process (RTP). It can operate at a low voltage for optimized power consumption (see datasheet TSC695FL). It has been specially designed for space, as it has on-chip concurrent transient and permanent error detection. The TSC695FL includes an on-chip Integer Unit (IU), a Floating Point Unit (FPU), a Memory Controller and a DMA arbiter. For real-time applications, the

TSC695FL offers a high security watchdog, two timers, an interrupt controller, parallel and serial interfaces. Fault tolerance is supported using parity on internal/external buses and an EDAC on the external data bus. The design is highly testable with the support of an On-Chip Debugger (OCD), and a boundary scan through JTAG interface. The TSC695FL is a selection of the TSC5695F performed for a narrow 3.3V biasing voltage range (± 0.15V), as such, this specification can be only met by the products solds as TSC695FL. Where computing power is not the key factor, it allows for a dramatic power consumption reduction (70%).
ATF697FF is a multichip module integrating a 32 bit RISC processor together with a reconfigurable unit. The processor implementation is the European Space Agency (ESA) SPARC V8 LEON2 fault tolerant model also known as AT697F for the Atmel standalone chip. The reconfigurable unit is based on the Atmel 280kgates radiation hardened SRAM-based reprogrammable FPGA also known as ATF697FF.

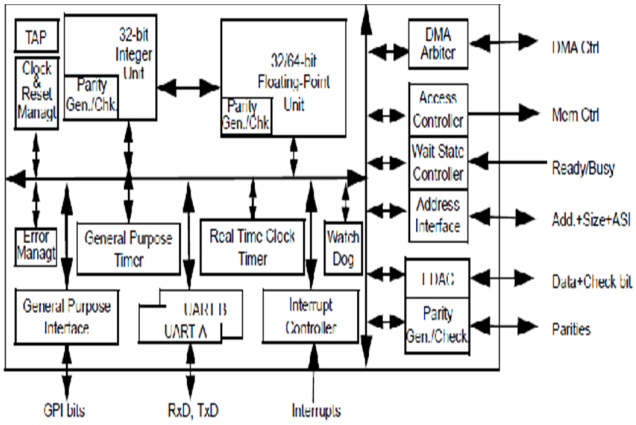

Figure 3: Block diagram of TSC695FL

Both the processor unit and the reconfigurable units are manufactured using the Atmel 0.18µm rad-hard AT58KRHA CMOS technology. The two dies have been especially designed for space application by implementing hardened cells, on-chip concurrent transient and permanent error detection and correction and permanent self integrity check mechanism.
ATF697FF contains an on-chip Integer Unit (IU), a Floating Point Unit (FPU), separate instruction and data caches, hardware multiplier and divider, interrupt controller, debug support unit with trace buffer, two 32-bit timers, Parallel and Serial interfaces, a Watchdog, a reconfigurable unit, a flexible Memory Controller and a 280 K gates of reconfigurable unit (fig.4). The configurable unit embeds 8 global clocks, 2 high speed clocks, 4 LVDS interface and 140 cold sparing and PCI compliant programmable I/Os dedicated to the application needs. The communication between the processor and the reconfigurable unit is performed by three different means: the internal PCI interface, GPIO and the EBI interface. ATF697FF only requires memory to be added to form a complete on-board computer.

B. ARM Processors

ARM Cortex-A9 MPCore™ processor: A multicore processor that delivers the second generation of the ARM MPCore technology for increased performance scalability and increased control over power consumption. The Cortex-A9 processor provides unprecedented levels of performance and power efficiency making it an ideal solution for any design requiring high performance in a low-power, cost sensitive, single processor based device. Using a convenient synthesizable flow and IP deliverables, the Cortex-A9 processor provides an ideal upgrade path for existing ARM11™ processor-class designs that require higher performance and increased levels of power efficiency within a similar silicon cost and power budget while maintaining a compatible software environment.

C. LEON Processors

The LEON 3 is a 32 bit processor based on the SPARC V8 architecture with support for multiprocessing configurations. The processor is fully synthesizable and up to 16 CPU cores can be implement in asymmetric multiprocessing (AMP) or synchronous multiprocessing (SMP) configurations.
A typical configuration with four processors is capable of delivering up to 1400 Dhrystone MIPS of performance. The LEON3 multiprocessor core (fig.6) is available in full source code under the GNU GPL

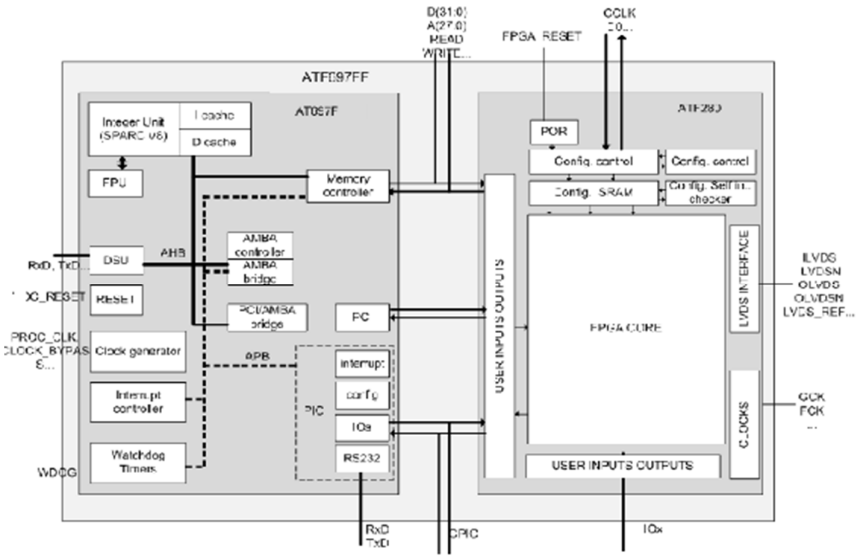

Figure 4: Block diagram of ATF697FF

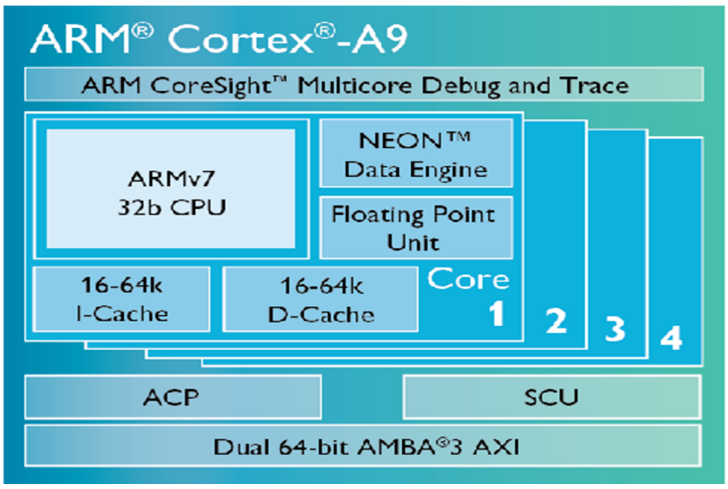

Figure 5: Block diagram of ARM Cortex A9 Multicore Processor

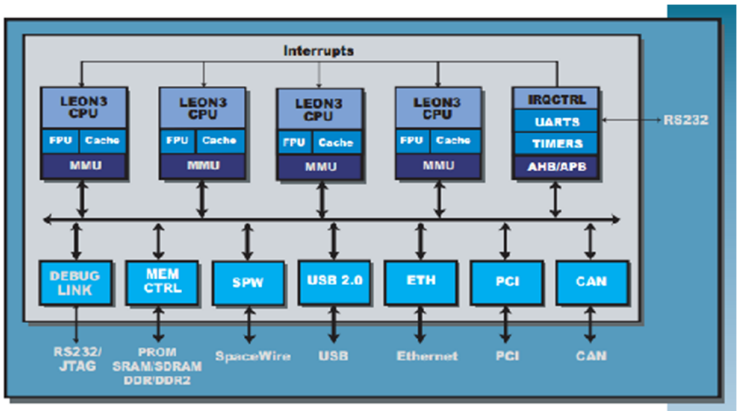

Figure 6: Block diagram of LEON 3 Processor

license for evaluation, research and educational purposes. A low cost license is available for commercial applications. LEON3 can be utilized in both SMP and AMP configurations. The processor provides hardware support for cache coherency, processor enumeration and interrupt steering. A unique debug interface allows non-intrusive hardware debugging of both single- and multi-processor systems, and provides access to all on-chip registers and memory. Trace buffers for both instructions and AMBA bus traffic are also available. An AMBA round-robin arbiter provides fair bus utilization for the processors.

The LEON3FT is a fault-tolerant version of the standard LEON 3 SPARC V8 processor.. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories.

The LEON3FT-RTAX processor is a SOC design based on LEON3FT core, implemented in the RTAX2000S radiation-tolerant FPGA. The processor is delivered as a programmed and tested RTAX2000S device, with several package and quality options. The combination of the RTAX2000S radiation-tolerance and the fault-tolerant capabilities of LEON3FT makes LEON3FT-RTAX suitable for any space application. To validate the fault-tolerance properties of the LEON3FT-RTAX design, a heavy-ion error-injection test campaign was carried in November 2005. The test was fully successful and confirmed the suitability of the LEON3FT-RTAX processor for critical space applications The LEON4 processor core is a synthesizable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The core is highly configurable and particularly suitable for high performance multi-core system-on-a-chip (SOC) designs. The core is interfaced using the AMBA 2.0 AHB bus and supports the IP core plug & play method provided in the Aeroflex Gaisler IP library (GRLIB). The processor can be efficiently implemented on FPGA and ASIC technologies and uses standard synchronous memory cells for caches and register file. The processor supports the MUL, MAC and DIV instructions and an optional IEEE-754 floating-point unit (FPU) and Memory Management Unit (MMU). The LEON4 cache system consists of separate I/D multi-set Level-1 (L1) caches with up to ways per cache, and an optional Level-2 (L2) cache for increased performance in data intensive applications. The LEON4 pipeline uses 64-bit internal load/store data paths, with an AMBA AHB interface of either 64- or 128-bit. Branch prediction, 1-cycle load latency and a 32x32 multiplier results in a performance of 1.7 DMIPS/MHz, or 2.1 Coremark /MHz.

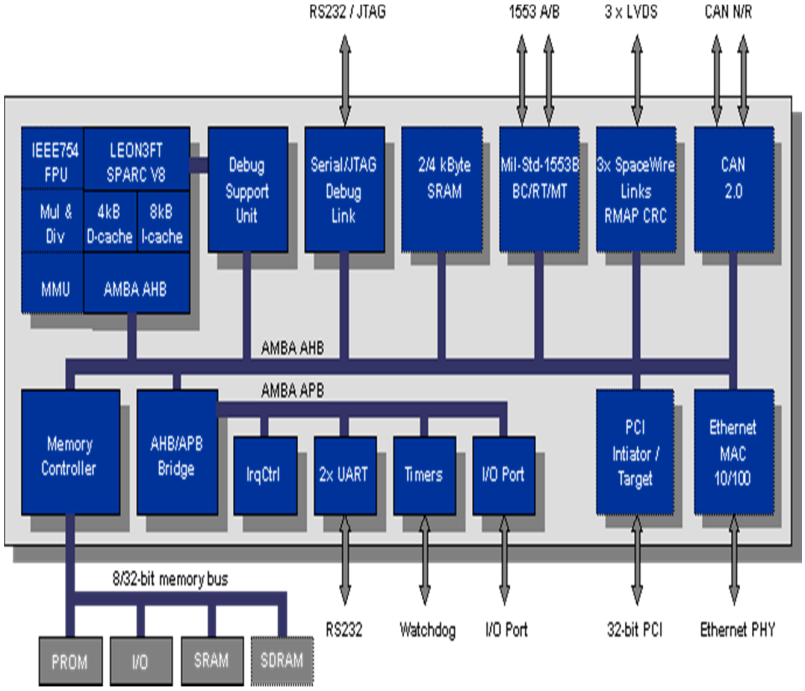

Figure 7: LEON3FT-RTAX Processor

On the basis of survey we proposed a roadmap of processors that can be studied from table I which will be beneficial for researchers and developers doing their work in this area.

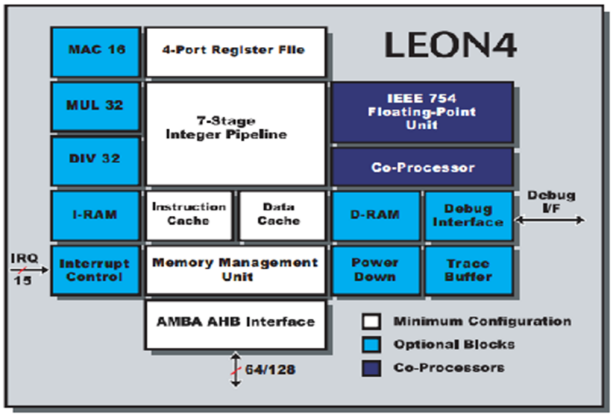

Figure 8: LEON 4 Processor

TABLE I: COMPARISON ANALYSIS OF VARIOUS PROCESSORS

Processors	Application Domain	Temperature Range	Operating Voltage	Single event Latchup (SEL)	Performance	Applications
AT697	32 bit high performance low power processor with SPARC V8 architecture	-55ºc to 125ºC	3.3V +/0.30V for I/O 1.8V +/0.15V for core	No SEL below a LET threshold of 80Mev/mg/cm^2	86MIPs/23MFLOPs	High Performance Applications
TSC695F	Integrated unit based on SPARC V7 high performance RISC architecture	-55ºc to 125ºC	4.5V to 5.5V	No SEL below a LET threshold of 80Mev/mg/cm^2		Real Time Applications
TSC695FL		-55ºc to 125ºC	3.15V to 3.45V	No SEL below a LET threshold of 80Mev/mg/cm^2	12MIPs/3MFLOPs	Embedded space application
ATF697FF	SPARC V8 High Performance Low-power 32-bit processor core	-55ºc to 125ºC	3.3V+/0.30V for I/O. 1.8V+/0.15V for core. 1.25V +/0.15V for LVDs reference	No SEL below a LET threshold of 60Mev/mg/cm^2 at 125°C.	86MIPs/23MFLOPs	
CORTEX A9		-55ºc to 125ºC				Networking and Mobile Applications
LEON3		-55ºc to 125ºC			1400 DMIPS	Nuclear power Plant, medical Electronics, High altitude avionics
LEON3 FT RTAX		-55ºc to 125ºC	1.5V to 3.3V			Payload and spacecraft control applications
LEON4	Synthesizable VHDL model of 32 bit processor with SPARC V8 architecture	-55ºc to 125ºC	1.8V		1.7 DMIPS/MHz, or 2.1 Coremarks /MHz.	Space Applications but not suitable for harsh environment.

IV. CONCLUSIONS

In this paper survey of various space processors is presented and discussed. Included are the architecture, design technology, performance, applications etc. On the basis of survey we present a roadmap of processor.

Based on the rapid advancement in this interesting research area we added several new updates of processors compared to the prior surveys.

On the basis of survey, we conclude that there is a great need to develop more reliable processors and with new technology.

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